FEI4 Collaboration

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Motivation for New Pixel Detector FE chips

- FEI4: novel ATLAS pixel detector readout chip for higher luminosity LHC phases
- Performance of present innermost pixel layers degrades with increased pile-up
  - Need replacement to maintain/improve tracking performance
- Build innermost layer closer to interaction point and use less material
- LHC luminosity upgrade (Phase I) targets to \( L = 2 \times 10^{34} \text{cm}^{-2}\text{s}^{-1} \) by 2020
  - Need fast front-end electronics to reduce dead-time
  - Improve radiation hardness of readout electronics and sensors

**ATLAS: pixel detector upgrade in 2 steps**

- **IBL (2013):** Add 4\textsuperscript{th} pixel layer at 3.2cm radius to existing pixel detector
- **New pixel detector for HL-LHC**
  - FEI4 fulfills design requirements for outer layers
Key Features of FEI4

• Designed to cope with higher hit rate
  – Regional architecture
  – Smaller pixel size
• Improved cost effectiveness
  – Big chip
  – Greater fraction of footprint devoted to active area
• No need for module control chip
  – Significant digital logic in periphery
• Lower power
  – Improved design and architecture
• Increased radiation tolerance (up to 250Mrad)
  – 130nm technology

FEI4 compared to its predecessor FEI3

<table>
<thead>
<tr>
<th></th>
<th>FEI4B</th>
<th>FEI3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Year</td>
<td>2011</td>
<td>2003</td>
</tr>
<tr>
<td>Technology</td>
<td>130nm</td>
<td>250nm</td>
</tr>
<tr>
<td>Chip size</td>
<td>20x19mm$^2$</td>
<td>7.6x10.8mm$^2$</td>
</tr>
<tr>
<td>Active area</td>
<td>89%</td>
<td>74%</td>
</tr>
<tr>
<td>Array</td>
<td>80x336</td>
<td>18x160</td>
</tr>
<tr>
<td></td>
<td>(26’880)</td>
<td>(2’880)</td>
</tr>
<tr>
<td>Pixel size</td>
<td>50x250μm$^2$</td>
<td>50x400μm$^2$</td>
</tr>
<tr>
<td>Number of transistors</td>
<td>87M</td>
<td>3.5M</td>
</tr>
<tr>
<td>Data rate</td>
<td>320 Mb/s</td>
<td>40Mb/s</td>
</tr>
<tr>
<td>Wafer yield</td>
<td>60%</td>
<td>80%</td>
</tr>
</tbody>
</table>
FEI4 Building Blocks

- Pixel digital regions (PDR) serving 4 analog pixels
  - 13-bit memory for each pixel
- Global EODCL, EOCHL, DOB
- Clock Generation
  - 40, 80, 160, 320 MHz
- Two configuration modes
  - CMD
  - Bypass configuration
  - Configuration Registers
- Power
  - Direct
  - Voltage regulator
- Bias DACs and CREF
- EFUSE
FEI4 Development

• **FEI4A: First full scale chip submission in July 2010**
  – 16 wafers (first wafer received in September 2010)
  – Chip thoroughly tested in 2010/11
    – Wafer probing, single chip tests, irradiation
  – First FEI4 based bump-bonded modules in January 2011
    – Lab tests, irradiations, operation in testbeams, cosmic data taking
  – Very successful project
    – Made accelerated timescale of IBL project possible

• **FEI4B: Production chip for IBL**
  – Chip submission in September 2011
    – Only minor modifications with respect to FEI4A
    – Added functionality to meet IBL DAQ requirements
  – First chips received in December 2011
    – Wafer probing, testing, irradiation, first modules available

• **FEI4C: Adapt FEI4 for outer layers of ATLAS pixel detector upgrade**

• **FEI4 design serves as basis for future chip design in 65nm technology, 3D technology**
## From FEI4A to FEI4B

- No changes needed for main components
  - Analog pixel, PDR, EODCL, CMD, DOB, CLK GEN
- New logic:

<table>
<thead>
<tr>
<th>Added functionality in EOCHL</th>
<th>Additional blocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increased trigger and BC counter, event truncation, skipped trigger counter, fixed shift register readback</td>
<td>Measurement circuit for injection capacitances, GDAC, temp sens, analog mux</td>
</tr>
</tbody>
</table>

- Modular design of the chip facilitates changes and additions
- Need for detailed verification in simulation of new and complex functionalities (together with the existing ones)
- Functional verification based on digital model of the full chip
- Verilog netlist generated directly from top-level schematic
- Tested from configuration, data flow, event and trigger management, exception handling to full physics simulation
- Invaluable tool for debugging
Column Design

- FEI4A has columns with different comparator, feedback capacitance and latch design for performance studies.
- Baseline column with metal-metal feedback capacitance and classic comparator chosen for FEI4B.

SEU rate measurement performed at CERN SPS

- Use of pixel latch design developed at CPPM significantly improves SEU hardness (by factor 30).
FEI4B for IBL

• Two different types of silicon sensor technologies used in IBL
  – 2-chip modules for planar n-in-n sensor
  – Single chip modules for partial 3D sensor

• IBL specifications
  – In-time threshold <4000e with dispersion <100e
  – Average hit rate with <1% data loss 40 MHz/cm²
  – Maximum trigger rate 200kHz
  – Data output rate 160Mb/s

• Powering scheme
  – VDDA = 1.2-1.5V, VDDD = 1.2V
  – 2 in-chip LDOs for analog and digital supply
  – In-chip regulators in partial shunt mode
  – Different reference voltage options (band gap or tunable reference voltage)

⇒ for more information on IBL modules see Martin Kocian’s presentation
Reference Voltage Options

- Reference voltage generation is new feature in FEI4B
- Fixed voltage reference: $V_{\text{ref}} = V_{\text{out}}/2$
  - Band gap reference increases with irradiation
  - Possible danger to FE if VDDA increases above 1.5V
- Tunable voltage reference
  - Generated from $I_{\text{ref}}$ which is powered from analog regulators
  - Leads to startup issues at low temperatures
Powering Scheme for IBL

- Tunable and fixed $V_{\text{ref}}$ tied together for analog regulator
  - Additional startup current leads to safe power up at low temperatures (tested down to -60°C)
  - Provides good tuning range
  - $V_{\text{ref}}$ can be set low enough to ensure safe operation even after irradiation

- Tunable $V_{\text{ref}}$ used for digital regulator
  - No start-up issues since $I_{\text{ref}}$ is powered from analog regulators
Regional Memories in FEI4

- Pixel digital regions (PDR) process data from 4 analog pixels
- Clock distributed to all PDRs to allow for ToT measurement
- Hits are stored locally during L1 latency
  - 5 ToT memories per pixel, 5 latency counters per region
- Hits are not moved unless triggered
  - Lower digital power consumption (6μW/pixel at IBL occupancy)
- Use spatial association for digital timewalk correction
FEI4 High Rate Capability

• Regional architecture of FEI4 overcomes rate limitations present in FEI3’s column drain architecture

Simulated inefficiency at radius $r = 3.7$ cm as a function of the number of pile-up events per 25ns

Column drain architecture saturates

Scales with number of counters per region

Scales with pixel area
Digital Column Simulation vs Measurement

Simulation @ 1.2V

Average power for 4-pixel region at IBL occupancy (MC hits)

<table>
<thead>
<tr>
<th>simulation type</th>
<th>avg power [uW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>ETS$^1$</td>
<td>42.28</td>
</tr>
<tr>
<td>Spectre</td>
<td>25.19</td>
</tr>
<tr>
<td>Ultrasim (s)</td>
<td>24.69</td>
</tr>
<tr>
<td>Ultrasim (a)</td>
<td>24.73</td>
</tr>
<tr>
<td>Ultrasim (ms)</td>
<td>35.12</td>
</tr>
<tr>
<td>HSIM$^1$</td>
<td>27.64</td>
</tr>
<tr>
<td>HSIM</td>
<td>30.98</td>
</tr>
</tbody>
</table>

$^1$ Parasitic extraction done with PEX

Measurement @ 1.2V

Occupancy faked with periodic charge injections

Power per region [uW] vs Fraction of occupied counters

Approximate IBL range

Lea Caminada

VERTEX 2012
FEI4 Analog Pixel

- Two-stage amplification
- Comparator with global and local threshold adjustment (TDAC)
- Global and local feedback current adjustment (FDAC)
- ToT counters within pixel digital region

<table>
<thead>
<tr>
<th></th>
<th>FEI3</th>
<th>FEI4</th>
</tr>
</thead>
<tbody>
<tr>
<td>ToT</td>
<td>8 bit</td>
<td>4 bit</td>
</tr>
<tr>
<td>TDAC</td>
<td>7 bit</td>
<td>5 bit</td>
</tr>
<tr>
<td>FDAC</td>
<td>3 bit</td>
<td>4 bit</td>
</tr>
</tbody>
</table>

FEI4 analog pixel diagram:

- Preamp
- Amplifier
- Comparator
- Feedback current adjustment (FDAC)
- ToT threshold adjustment (TDAC)
- HitOut
- NotKill

Lea Caminada
VERTEX 2012
Threshold Dispersion

- Tuned threshold dispersion \( \sim 30e \)
- FEI4 low threshold operation (~1400e) shows promising results with reasonable dispersion
- Irradiation tests with bare chips show no effect on threshold dispersion
Noise

• Noise measurement before and after proton irradiation up to 200 Mrad
• Absolute value of noise is \(~100e\) without sensor load
• Noise increases by about 20% after irradiation
Charge Calibration

- 4-bit ToT for charge measurement
- Pulse gen circuit and injection capacitance to simulate charge injection
- Simulated capacitance is 5.7fF with large uncertainty
- FEI4A: indirect measurement of charge calibration based on source scan data (uncertainty due to unknown charge collection efficiency)
- FEI4B: Direct measurement of injection capacitance using dedicated circuit. Mean cap = 6fF, spread = 5.5-6.8fF.
Wafer Probing

IBL production wafer tests performed in Bonn

Chip calibrations
Reference current tuning
Charge calibration
15-bit serial number burning

Global IC tests
Current consumption
$V_{\text{ref}}$ setting
Global configuration
Functionality of digital periphery
Scan chains
Injection delay circuitry

Pixel Array tests
PDR:
hit processing, buffering, latency counters
Analog performance:
Analog test, threshold, noise

Aptasic tests
IDDQ tests
Scan chains
Shmoo plots
Current consumption
Wafer Probing Results

- **Current reference tuning**
  - Specification is 2μA
  - Measure centered distribution with 0.02μA RMS

- **Analog performance**
  - No threshold tuning performed during wafer probing → large spread in mean threshold
  - Noise performance as expected
Wafer Yield

• Preliminary average yield: 61%
• Main failure modes:
  23%: total pixels fail (>0.2% of all pixels show errors during scans)
  9%: run aborted (too high current)
  11%: measured currents outside nominal range
Conclusion

• FEI4 presents a new chip for pixel upgrade projects

• Includes real innovation and a novel readout architecture that reduces that power and also scales to higher rates

• Reduces the cost of module production due to its large size and reasonable high wafer yield

• Successful design of FEI4B for IBL (first production version of the chip)

• Design of FEI4 as baseline for future pixel chips using advanced technologies
Backup
FEI4 4-pixel digital region with neighbor logic
FEI3 Column Drain: Limitations at high rate

- **r=5cm at L=10^{34}\text{cm}^{-2}\text{s}^{-1}**
- **r=3.7\text{cm at } L=2\times10^{34}\text{cm}^{-2}\text{s}^{-1}**
Power Consumption

• FEI3
  – **Analog**: $75\text{mA} \times 1.6\text{V} = 120\text{mW/chip}$ => $21\mu\text{W/cm}^2$
  – **Digital**: $49\text{mA} \times 2.0\text{V} = 98\text{mW/chip}$ => $17\mu\text{W/cm}^2$

• FEI4
  – **Analog**: $350\text{mA} \times 1.2\text{V} = 420\text{mW/chip}$ => $10\mu\text{W/cm}^2$
  – **Digital**: $160\text{mA} \times 1.5\text{V} = 240\text{mW/chip}$ => $6\mu\text{W/cm}^2$
  – Reduced analog current in FEI4 (reduced analog performance is recovered by adding digital functionality)
  – Reduced digital current due to improved architecture
Noise for FEI4B with sensor connected
Complete list of changes FEI4A → FEI4B

- Fix problems discovered during FEI4_A testing:
  - Adjust range of selected bias DACs
  - Center CREF
  - Lower PulseGEN output impedance
  - Polarity of EFUSE reset
- Design choices for uniform pixel array
- Internally connect voltage regulators
- Rout power to the top pads from VDDA
- Add copy of the analog MUX to the bottom of the chip
- Add GDAC and tempsense circuit
- Add circuit for measurement of injection capacitances
- Improve SEU hardness of CONFIGMEM
- Add third prompt radiation detector (PRD) and increase threshold
- Modifications to EOCHL
  - Fix for SR readback, small hit suppression logic, increased LV1 and BCID counters, programmable event truncation, skipped trigger counter
Latches pixel implementation 1/2

- **FEI4_A**: 336 lines x 80 columns = 26880 pixels x 13 latches per pixel = 349440 configuration latches of pixels
- **There are 2 kinds of latches inside this chip:**
  - **Version A**: DICE latch structure with linear NMOS and PMOS implemented in 30 double columns
  - **Version B**: DICE latch issue to SEU chip using enclosed NMOS, PMOS linear and guard ring are implemented in 8 double columns
  - We extract this last version latches from previous SEU measurements we did at CERN with a dedicated chip

September 27th 2011

Vienna TWEPP 2011 – SEU WG
Time-walk Correction

- Small hits are associated to big hits based on position rather than on time information.
- PDR triggers on “big” hits and uses a time window of 2 BX to look for “small” hits.
- Allows for lower power operation since digital logic corrects for reduced analog performance.

![Graph showing ATLAS MC simulation with big and small hits]

![Graph showing Time-walk measurement in FEI4 with VCAL vs. Delay]
FEI4 Powering Scheme

- Regulator needs $V_{ref} = \frac{1}{2} V_{out}$.
- Two Options:
  - Bandgap reference.
  - Tuneable $V_{ref}$ from $I_{ref}$. 

Diagram:
- LDO
- $V_{out}$
- $V_{in}$
- $V_{ref}$
- $V_{ref \text{ bandgap}}$
- $V_{ref \text{ tune}}$
- $0.5 \times V_{out}$
- Tuneable $V_{ref}$ generation
- $I_{ref} = 2 \mu A$
FEI4A DC-DC converter: Test Results

Ideally, $I_{out} = 2 \times I_{in}$, $V_{out} = 1/2 \times V_{in}$.

$V_{in} = 3.3V$, $R_{load} = 5 \Omega$

Efficiency vs Clock frequency

- Schematic simulation gives 90% efficiency, while measured efficiency is ~84% (need to verify in post layout simulation).

$R_{out}$ on irradiated chips

- $R_{out}$ does not change with irradiation!

Noise maps:
- Direct powered
- DC-DC powered

- Small increase in noise (noise increase seen in earlier test due to external noise introduced by setup)