Belle Tracker Upgrade

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Heidelberg University
on half of the DEPFET- and the SVD-Collaboration
VERTEX2012
Jeju, Korea
SuperKEKB/Belle2 Upgrade

• Accelerator Upgrade
  – luminosity increase by 40x: \(8 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}\)
  – nano-beam scheme: 10µm x 60nm cross-section
  – 10mm beam pipe radius

• Very high background → Belle Detector Upgrade
• Strips not possible due to high background → need pixels on inner layers
• DEPFET pixel detector “PXD”
  – monolithic sensor
  – 2 layers at 1.4cm and 2.2cm
  – unique: 75µm thin
  – self supporting all-silicon module
  – ~50x50µm² pixels
• Double Sided Strip Detector “SVD”
  – 4 layers at 3.8, 8.0, 10.5, 13.5 cm
  – slanted forward part
  – individual read-out, no daisy-chaining
**Vertex Tracker Improvement**

- **Belle2**
  - occupancy: 0.4 hits/µm²/s
  - radiation: > 1Mrad/year
  - avg. particle momentum: 500MeV
  - acceptance: 17°-155°

- **High vertex resolution required**
  - low material budget

New PXD+SVD improves z-vertex resolution by factor of 2
DEPFET Pixel Cell

• Signal generation in fully depleted bulk
  – fast & complete signal collection
• Integrated p-channel FET transistor
  – read-out amplification
  – low noise
• Deep n-implant accumulates electrons
  – “internal gate”
  – modulates transistor current
  – continuous signal collection
  – low power
• External gate to enable read-out
• Clear contact removes charge from internal gate
• Blind mode
  – existing charge in internal gate is conserved
  – new charge (injection noise particles) are drained in clear contact
Matrix Readout

- Row wise read out ("rolling shutter")
- Single sampling
  - faster readout
  - 100ns / row
  - entire PXD: 20µs (50kHz frame rate)
- **Switch gate and clear signals**
  - AMS 0.35µm HV
  - 3.6 x 2.1 mm²
• Drain Current Digitizer (DCD)
  - UMC 0.18µm 1.8V
  - 8-bit cyclic ADCs
  - 3.2 x 5 mm²

256 inputs
512 ADCs
80ns sampling

Power Supply
8x 8Bit data out
320MHz, 20GBit/s

Noise:
50nA, 100e
- **Data Handling Processor (DHP)**
  - hit finding & data reduction
  - switcher control
  - slow control hub (JTAG)
  - 3.3 x 4.2 mm²
  - NEW: successful communication with DCD

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**Diagram:**

- 10 MHz row frequency
- 100 ns ADC conversion time
- 256 inputs per DCD
- 8 bit ADC + 2 bit DAC per input
- 4:1 output mux
- 81.9 Gbps
- 320 Mbps output data x 256 lines
- 5 Gbps (1.25 Gbps link per DHP)

**Input from DCD**
- Power
- Data out, fast & slow control
- Data out,
- Input from DCD
- Power

**DCD**
- Deserializer
- Pedestal subtraction
- Common mode corr.
- FIFO 1
- Hit finder
- FIFO 2
- Framer
- Serializer

**DHP**
- PLL
- JTAG
- clock, sync
- one data out per DHP
- trigger
- raw data memory
- DAC memory
- pedestal memory
PXD Half Module

- PXD ladder is built of two half modules
  - module length restricted by wafer size
  - yield considerations

<table>
<thead>
<tr>
<th>Half Module</th>
<th>Inner layer</th>
<th>Outer layer</th>
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<tbody>
<tr>
<td># (half) modules</td>
<td>8 (16)</td>
<td>12 (24)</td>
</tr>
<tr>
<td>Radius</td>
<td>14 mm</td>
<td>22 mm</td>
</tr>
<tr>
<td>Pixel size</td>
<td>50x55 µm²</td>
<td>50x70 µm²</td>
</tr>
<tr>
<td></td>
<td>50x60 µm²</td>
<td>50x85 µm²</td>
</tr>
<tr>
<td>Thickness</td>
<td>75 µm</td>
<td>75 µm</td>
</tr>
<tr>
<td># pixels</td>
<td>1536(z) x 250(R-ϕ)</td>
<td>1536(z) x 250(R-ϕ)</td>
</tr>
<tr>
<td>Size</td>
<td>15x68 mm²</td>
<td>15x85 mm²</td>
</tr>
</tbody>
</table>
PXD DAQ

7.2GB/s
555MB/s
175MB/s

GbE

Event Builder

RocketIO

DHH

ATCA

40 readout units

DHH

ATCA

DCD Chips

DHP Chips

Kapton flex
50cm

250 x 768 pixel

~50μm

~75μm

drains

active area

cross section

1000 DCD channels
192 Gate and Clear

10-20m

10-20m

Slow Control (TWP)
Data Handling Hybrid
DHH

Optical

Optical

DHH Controller,
Trigger/Timing

JTAG

Slow Control

Power cables

Power Supply System

DAQ, data reduction,
ROI selection

20.09.2012 VERTEX2012: Belle Tracker Upgrade

Dr. Christian Kreidl
University of Heidelberg
PXD Module

- Glueing of half modules
- Slim support frame
- 75µm thin active area
- Flip chip directly onto detector, no interposer!
- Thick end outside acceptance!
- 0.18% $X_0$

Material budget distribution

- Sensitive
- Switcher
- Cu Layer
- Bumps
- Frame

Material budget studies: Belle II - SVD Barrel, PXD 75µm
PXD Mounting

- Kapton flex
- CO₂ inlets
- Positioning screw
- Cooling block
- Support ring
Thinned and glued silicon ladders
PXD Cooling

- Cooling system outside acceptance
- Closed CO2 cooling system for readout electronics (320W)
- Cold dry air for steering chips and DEPFET pixels (40W)

- Stainless steel
- Fast sintering
- Blue: CO2 channels
- Yellow: Air channels

Mockup with resistive heaters on silicon ladders

Free convection

Forced convection
**Thinning Technology**

1. implant backside on sensor wafer
2. bond sensor wafer to handle wafer
3. thin sensor side to desired thickness
4. process DEPFETs on top side
5. structure resist, etch backside up to oxide/implant

- 30% material reduction
- grooves for gluing

50µm → 75µm: resolution optimization

50µm thin
first thinned DEPFETs with 50µm thickness!
Lab Test & Testbeam

- **50µm thin DEPFETs**
  - 64x32 pixel, 50x75µm²
  - Belle2 design
- **Close to final ASICs**
  - full speed readout (100ns/row)
- **Find optimal DEPFET design for final production**
Testbeam Results

- Close to final steering and read-out chips

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Center of gravity residuals: \( \sim 18\,\mu m \)

\[
\frac{75\mu m}{\sqrt{12}} \sim 21\mu m
\]

Signal to Noise Ratio: \( \sim 35 \)

CERN Testbeam 2012

- 120 GeV \( \pi \)
- Normal incidence
- Landau fit
- SNR \( \sim 35 \)
- \( g_q \sim 500\,\text{pA/e}^- \)
• Belle software: no efficiency for low momentum tracks
  – new BASF2 framework, based on GEANT4, all subdetectors
• GENFIT / RAVE: track fitting with PXD, SVD, CDC
  – For online reconstruction of PXD data need to extrapolate CDC → SVD → PXD to find region of interest
• Everything except DEPFETs
  – Prototype of half ladder currently in production
  – 3 metal layers
  – Test: production, thinning, assembly, ASIC performance

- Switcher
- DCDB
- DHP
- Kapton connection

- Space for small DEPFET matrix
- Load capacitors for Switcher tests
First ever 50µm thin DEPFETs produced and perform well!
Final DEPFET pixel layout fixed
PXD geometries fixed
ASICS operate at final speed
CO2 cooling concept is working
Mechanical mockup with thin silicon modules
First full module layout with ASICS and kapton cable
Electrical Multi-Chip-Module in production
Test DAQ read out chain
Create final layout of PXD modules
Start production of final modules
Install PXD by mid of 2015

Research is funded by the Federal Ministry of Education and Research (BMBF)
Silicon Strip Vertex Detector ("SVD")
Old Belle SVD

- 4 layers of 4” double sided strip detectors
  - up to three sensors were daisy-chained
  - read out by VA1 chip on hybrid outside acceptance
  - 10% occupancy in innermost layer → faster shaping required
  - 3% dead time → faster readout required

Old SVD not suitable for Belle2
SVD for Belle2

- No daisy-chaining: Sensors are read out individually
- Layer 4-6 with slanted forward part
- Layer 3 with straight sensors
- Active CO2 cooling needed within acceptance
• AC coupled double sided read-out with poly-silicon biasing
• Rectangular: Hamamatsu; trapezoidal: Micron
• different p-stop layouts to evaluate optimum type and geometry

6 x 12 cm², 300µm thick

6” wafer with trapezoidal sensor
Beam Test Modules

2 sensors for tracking

3 DUTs

2 sensors for tracking

Baby Module for p-stop test
Test Beam Results

- 70Mrad gamma irradiation with Co-60
- CERN beam test before and after irradiation
  - Dark color: non-irradiated, Light color: irradiated
- Atoll pattern (half-wide) performs best
  - chosen for final sensor

```
<table>
<thead>
<tr>
<th>Geometry</th>
<th>Atoll p-stop</th>
<th>Common p-stop</th>
<th>Combined p-stop</th>
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<tbody>
<tr>
<td>narrow</td>
<td>30</td>
<td>35</td>
<td>30</td>
</tr>
<tr>
<td>half-narrow</td>
<td>35</td>
<td>30</td>
<td>25</td>
</tr>
<tr>
<td>half-wide</td>
<td>40</td>
<td>35</td>
<td>35</td>
</tr>
<tr>
<td>wide</td>
<td>35</td>
<td>30</td>
<td>25</td>
</tr>
</tbody>
</table>
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Atoll pattern (half-wide) performs best and is chosen for the final sensor.
Readout Chip APV25

• Developed for CMS (LHC) by Imperial College London and Rutherford Appleton Lab
• 0.25µm CMOS process (>100Mrad tolerant)
• 128 channels
• 192 cell analog pipeline
  – no dead time
• 50ns shaping time
  – low occupancy
• Multi peak mode
  – read out several samples along shaping curve
• Noise: 250e + 36 e/pF
  – Capacitive load must be minimized
• Successful thinning to 100µm

readout board with 4 thinned APV
Read Out System

• Analog data transmission up to FADC by copper cables
  – Signal conditioning using FIR filter
• Prototype read-out system exists
  – Verified in several test beams
  – Needs to be adapted for higher integration
• Possibility of recording multiple samples along waveform
• Reconstruction of peak time and amplitude
  – used to remove off time background hits

APV25 Hit Time Reconstruction

- Possibility of recording multiple samples along waveform
- Reconstruction of peak time and amplitude
  - used to remove off time background hits

Example graph showing signal over time with threshold and time over threshold.

- **VA1TA**
  - $T_p \sim 800\,\text{ns}$
  - Time over threshold ~ 2000\,ns (measured)

- **APV25**
  - $T_p \sim 50\,\text{ns}$
  - Time over threshold ~ 160\,ns (measured)
  - Gain $\sim 12.5$
  - Gain $\sim 8$
  - Total gain $\sim 100$
  - Pulse shape processing
  - $\text{RMS (max)} \sim 3\,\text{ns}$
  - Sensitive time window ~ 20\,ns

- Occupancy reduction
  - Belle → Belle2: x100
- Chip-on-Sensor concept for double-sided readout
- Flex fan-out wrapped to p-side ("Origami")
- All chips aligned on one side → single cooling pipe with $\text{CO}_2$

**Diagram:**
- 3-layer kapton hybrid
- APV25 chips (thinned to 100µm)
- Cooling pipe
- Fanout for n-side (z)
- Double-layer flex wrapped to p-side (r-phi)
- DSSD
- Top view
- Side view
Origami Module Assembly

backside gluing & wirebonding

module assembly

origami wrapping

finished assembly

unwrapped origami
Support ribs

Carbon fiber ribs and Airex foam: lightweight but strong sandwich

outermost layer
60 cm long

Average material over full module: 0.55 % $X_0$
Summary

• SuperKEKB will be the highest luminosity machine
  – 40-fold increase in luminosity relative to KEKB
• Belle detector upgrade (2010-2015)
  – all sub-detectors need upgrade
• New vertex detector
  – Two layers of DEPFET pixels
  – Four layers of double-sided strip detectors
• DEPFET
  – 75µm thin, low mass, self-supporting all-silicon modules
  – Final pixel geometry frozen, ASICs close to final
  – First electrical module layout in production
• Strip detector
  – Optimum p-stop geometry identified
  – Readout with hit time reconstruction for improved background tolerance
  – Origami chip-on-sensor concept for low mass readout
Thank you!
• high background → high radiation damage
  – Thresh. voltage shift of DEPFET is reduced from 25V to <5V with thin oxide
  – Segmented gate voltage to compensate inhomogenous voltage shifts
  – ASICs radiation hard

SwitcherB 3.3V: 24.5Mrad
SwitcherB 1.8V: Irradiation planned

DCD Testchip: 3.5Mrad
large DCD: Irradiation planned

DHP Testchip: SEU Measurements $10^{-3}$ bits/sec
**DEPFET gated mode**

- **Machine injection noise**
  - “noisy bunch” every 10µs → 2 passings per PXD readout frame
  - need to blind DEPFET when noisy bunch passes

- **New: gated mode operation**
  - keep already stored charge, direct junk charge into clear contact
  - charge all clear lines → high currents, need much decoupling
  - new steering chip in production

*normal mode: all trajectories into internal gate*

*blind mode: all trajectories into clear contact*

Software: Klaus Gärtner (WIAS)
Temperature distribution along the ladder

Reasonable environment conditions

\[ T_{\text{env}} = -5^\circ\text{C} \]
\[ T_{\text{cb}} = 8^\circ\text{C} \]

\[ T_{\text{max}} = 15.5^\circ\text{C} \]

- The end of the stave will be cooled by CO\(_2\) inside the cooling block
- The center will be cooled by blowing cold air

→ Both, SVD and PXD subdetectors will be thermally isolated from the CDC
Sensor Types

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<td>6</td>
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<td>64</td>
<td>16</td>
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<td>5</td>
<td>12</td>
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<td>12</td>
<td>480</td>
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<td>20</td>
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<tr>
<td>3</td>
<td>7</td>
<td>14</td>
<td>0</td>
<td>0</td>
<td>168</td>
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<tr>
<td>Sum:</td>
<td>49</td>
<td>14</td>
<td>120</td>
<td>38</td>
<td>1748</td>
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</table>
### Barrel Layout

<table>
<thead>
<tr>
<th>Layer</th>
<th>Sensors/Ladder</th>
<th>Origamis/Ladder</th>
<th>Ladders</th>
<th>Length [mm]</th>
<th>Radius [mm]</th>
<th>Slant Angle [°]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>2</td>
<td>0</td>
<td>7</td>
<td>262</td>
<td>38</td>
<td>0</td>
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<tr>
<td>4</td>
<td>3</td>
<td>1</td>
<td>10</td>
<td>390</td>
<td>80</td>
<td>11.9</td>
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<tr>
<td>5</td>
<td>4</td>
<td>2</td>
<td>12</td>
<td>515</td>
<td>105</td>
<td>16</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>3</td>
<td>16</td>
<td>645</td>
<td>135</td>
<td>21.1</td>
</tr>
</tbody>
</table>

**Images:**
- [Diagram of Barrel Layout](image1)
- [Diagram of Barrel Layout](image2)

**Key Components:**
- **Slanted Sensors**
- **Origami**
- **Cooling Tubes**
- **Hybrid Boards**
• Results achieved in **beam tests** with several different types of Belle DSSD prototype modules (covering a broad range of SNR)

• **2...3 ns RMS** accuracy at typical cluster SNR (15...25)

• Working on implementation in **FPGA** (using lookup tables) – simulation successful

![Time Resolution vs. Cluster SNR](image)

(tDC error subtracted)
- Power dissipation per APV: 0.40 W
- 1 Origami sensor features 10 APVs

<table>
<thead>
<tr>
<th>Origamis /Ladder</th>
<th>Ladders</th>
<th># APVs Origami</th>
<th># APVs Hybrid</th>
<th>Power/ Layer [W]</th>
<th>Power Origami [W]</th>
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<tbody>
<tr>
<td>Layer 6</td>
<td>3</td>
<td>16</td>
<td>480</td>
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<td>320</td>
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<td>Layer 5</td>
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<td>240</td>
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<td>Layer 4</td>
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<td>200</td>
<td>120</td>
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<td>0</td>
<td>140</td>
<td>56</td>
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<tr>
<td>Sum</td>
<td>47</td>
<td>820</td>
<td>900</td>
<td>688</td>
<td>328</td>
</tr>
</tbody>
</table>

- Total Origami power dissipation: 328 W
- 360 W dissipated at the hybrid boards
- Total SVD power dissipation: 688 W