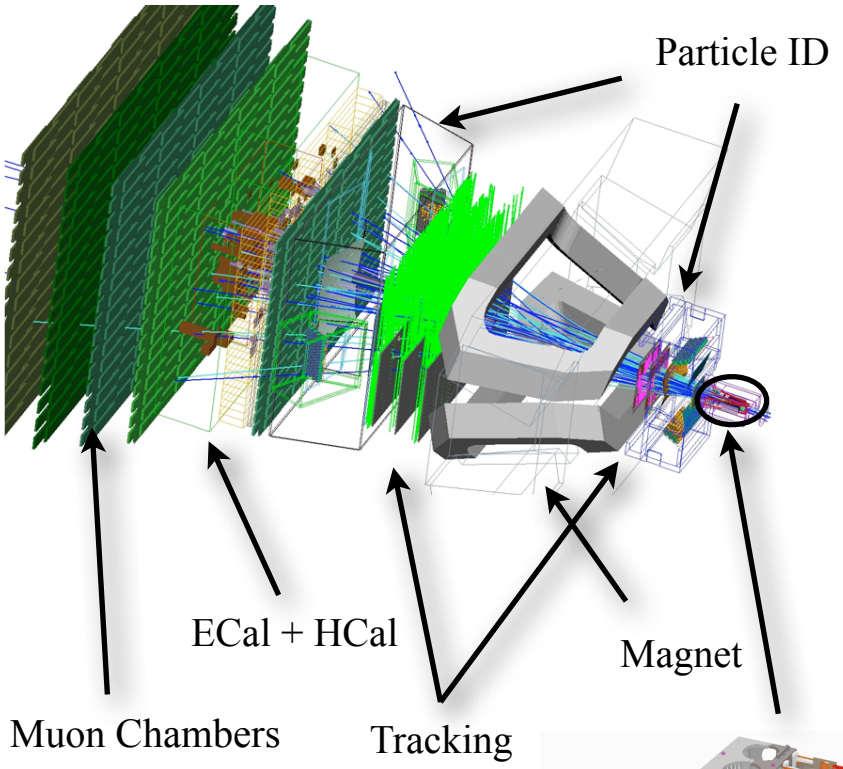
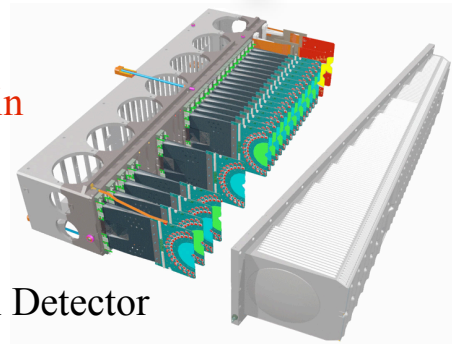
The LHCb VELO Upgrade

Daniel Hynds
(On behalf of the LHCb Collaboration)

Current detector overview

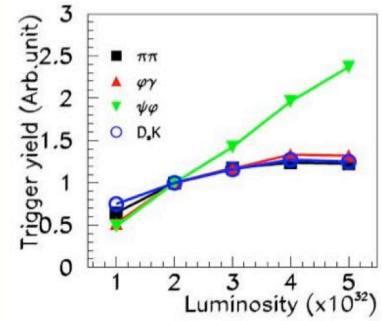


Overview in talk by Mark Tobin



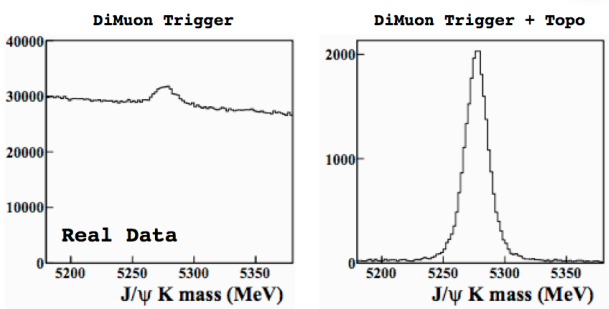
Vertex Detector

- Flavour physics experiment built to cover forward geometry
- Design luminosity lower than LHC deliverable
  - Built for $\mathscr{L} = 2\times10^{32}$ cm^2 s^{-1} at 25ns spacing (interaction per bunch crossing $\mu = 0.4$)
  - Currently operating at $\mathscr{L} = 2 - 4\times10^{32}$ cm^2 s^{-1} at 50ns spacing ($\mu = 1.4 - 1.7$)
- Running at higher luminosity does not improve hadronic event yield due to trigger bottleneck

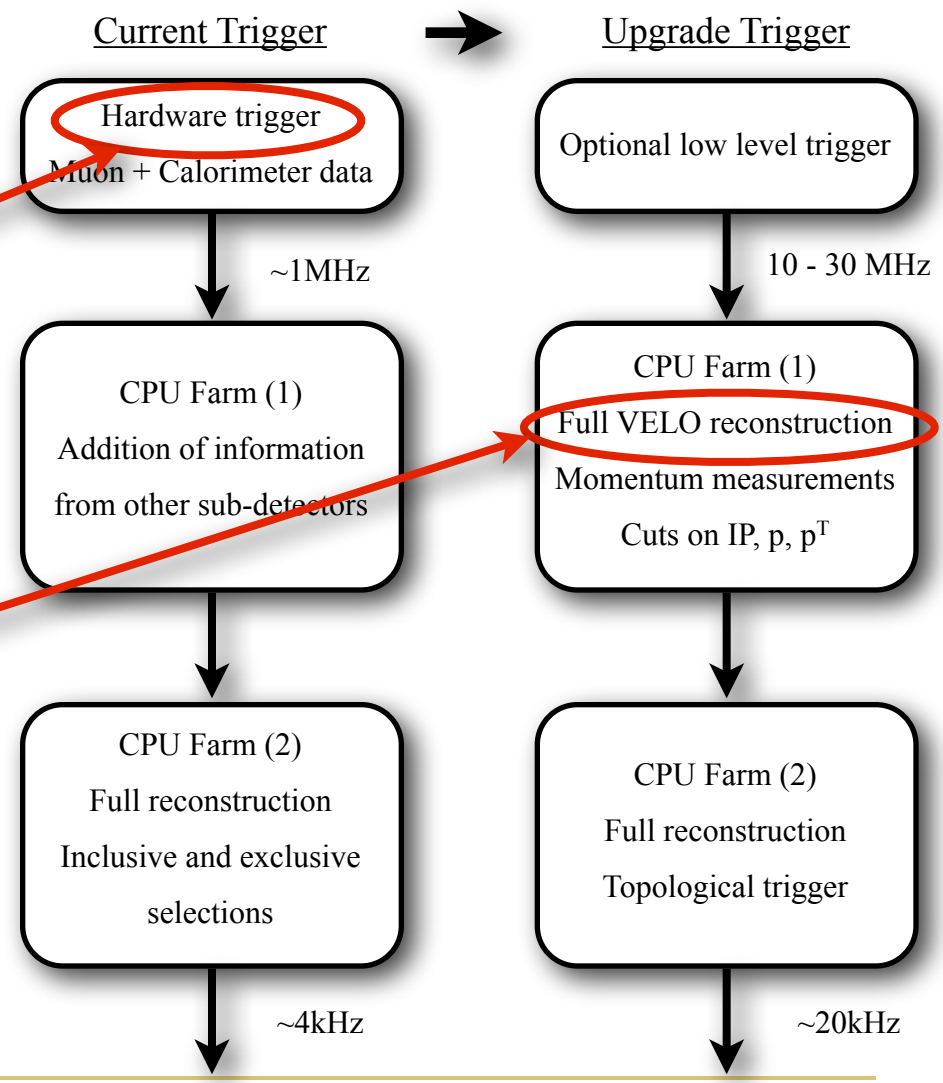


LHCb upgrade

- Why upgrade? **Triggering**
- Hardware trigger limits efficiency in hadronic modes
  - Turning up the luminosity doesn't translate to increase in interesting in events
  - Remove hardware trigger
  - Luminosity increase gives factor 10 improvement to muonic channels, 20 to hadronic channels (not possible with current trigger)
- Move triggering completely to software for full flexibility
  - Reconstruct all events at 40MHz



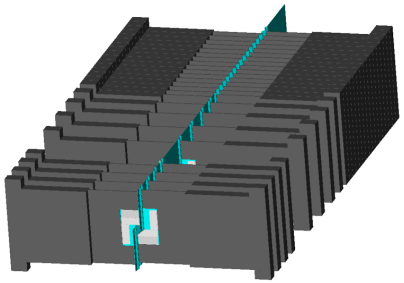
Comparison of **hardware** trigger (left) with **Topological** (right)



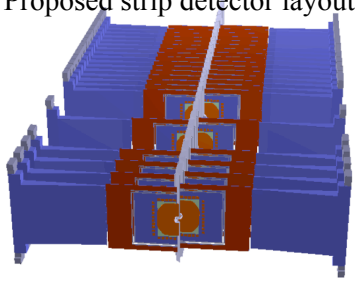
VErtex LOcator (VELO)

- **Present detector** was a huge accomplishment:
  - High IP resolution
  - 1MHz readout
  - Clean reconstruction
- Effective design:
  - Single sided n^+-on-n silicon sensors
  - Each half-station contains an R- and Φ- sensor
  - Mounted in secondary vacuum, separated from beam vacuum by 300μm RF foil
  - Mobile: mechanically moved from 30mm to 8mm for data taking

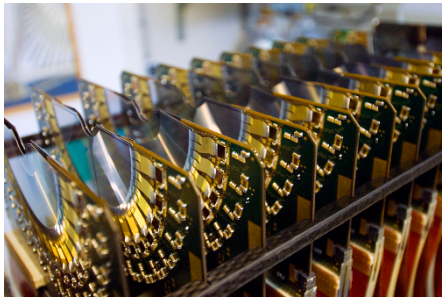
Proposed pixel detector layout

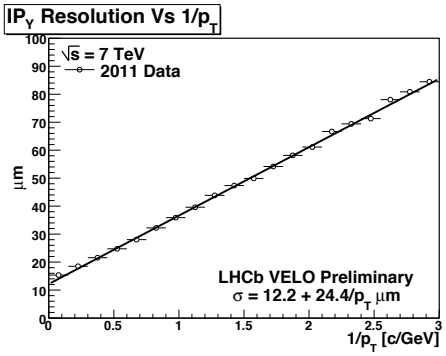


Proposed strip detector layout



- **Future detector** must improve on this:
  - Increase readout to 40MHz for full reconstruction
  - Increase granularity to allow operation at $\mathscr{L} = 2\times10^{33}$ cm^2 s^{-1}



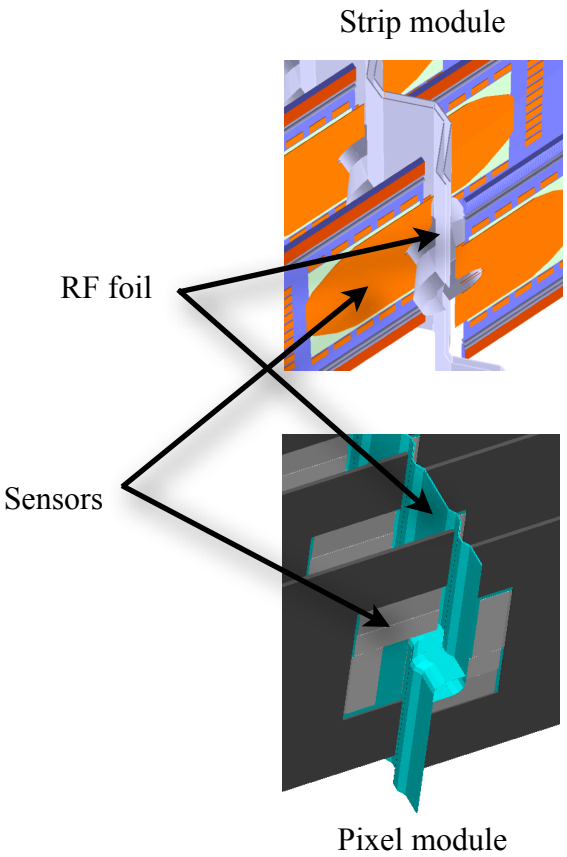


- 2 options proposed
  - Strip detector following similar philosophy to existing design
  - Pixel detector based on TimePix family of chips

Module Overview

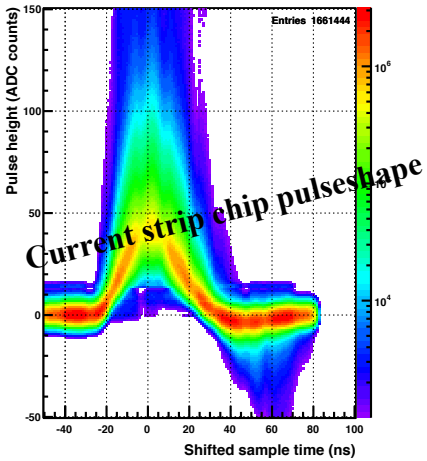
- For both detector proposals, module design based along similar ideas
  - Move to 200µm n-on-p sensors (single sided processing)
  - High thermally conductive spine - diamond proposed as strong candidate, or silicon microchannels
  - Re-use of existing infrastructure - CO_2 cooling plant, vacuum vessel, motion system
  - Completely new RF foil

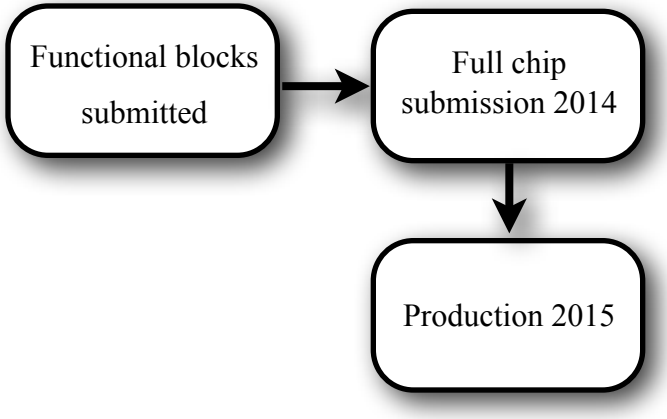
- Notable module differences
  - Strip option keeps dead material at the periphery of the measurement area (out of acceptance)
  - Pixel option uses single layer of flip chip assemblies per module, mounted on both faces of the cooling spine to allow a small overlap between ASICs and optimise mechanical stability.



Strip detector front end

- Front end chip currently being designed, with overlap between VELO and tracking stations
- Chip specifications (50ke$^-$ signal)
  - ~25ns peaking time
  - Zero suppressed output
  - Sampling tuneable in 0.5ns steps over full 25ns range
  - Signal 25ns after peaking < 5%
  - Recovery within 10 bunch crossings
  - 6-bit on chip ADC
- Sensors are designed with varying strip pitch such that occupancy is even amongst all strips => modest data rate requirements (1.4 Gbit s^{-1})

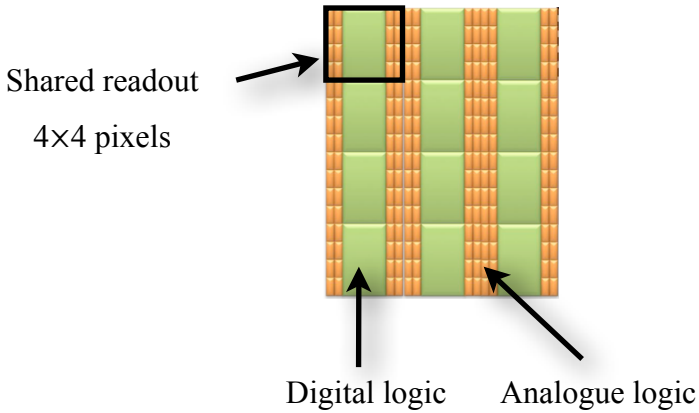


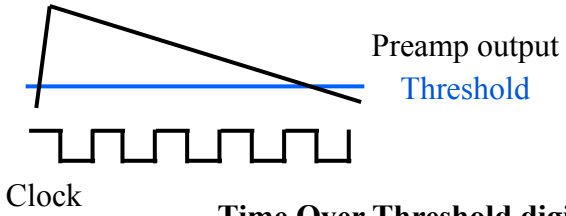


- Required functionality:
  - Take advantage of 130nm process - move signal processing on-chip
  - Common mode supression
  - Pedestal subtraction
  - Strip masking
  - COG Clustering? Or aim for simplicity...?

Pixel detector front end

- Chip specifications
  - 55μm × 55μm pixels
  - 4+ bit ToT counter size
  - 12-bit bunch crossing counter
  - < 25ns timewalk at 1ke$^-$
  - 50ke$^-$ dynamic range (tuneable)
  - **Hit rate 500 MHz**
  - Power consumption < 3W
  - **Output bandwidth > 12 Gbit s^{-1}**
  - **Data driven readout (not triggered)**



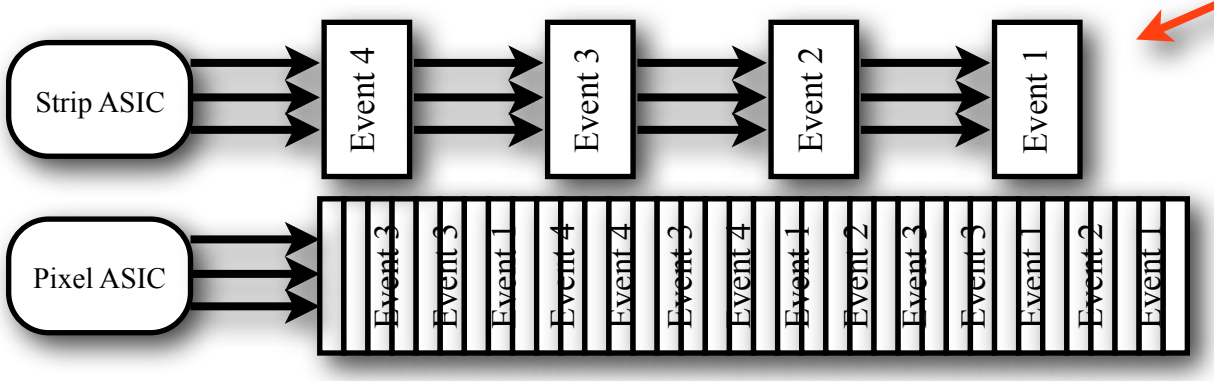


Time Over Threshold digitisation combined with data driven readout => pixel busy time proportional to deposited charge

- Chip designed around the TimePix family of chips
- Digital logic shared between neighbouring pixels
  - => On-chip data compression
  - All hits in a 4×4 region from the same bunch crossing read out together

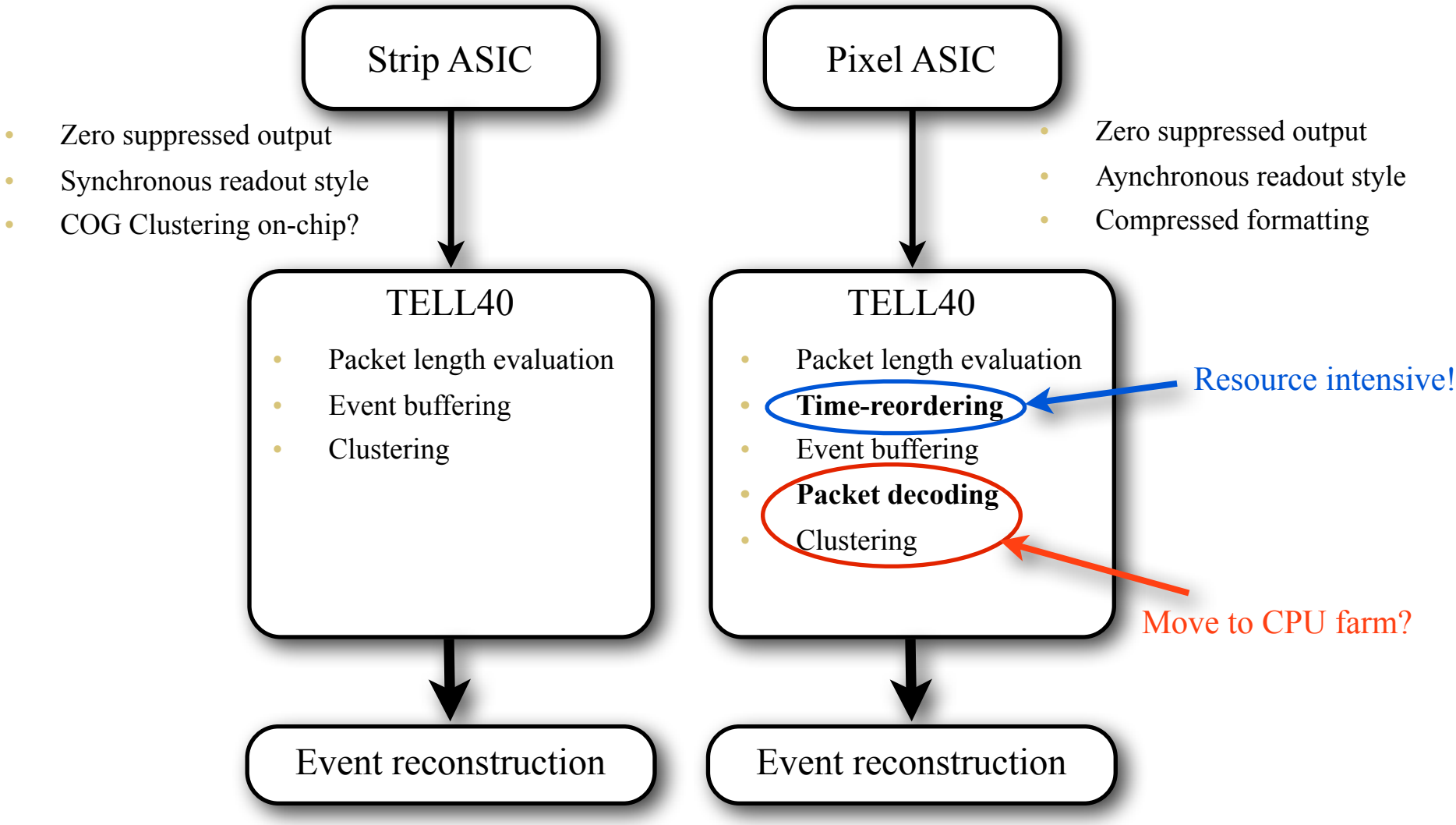
Data rates

- For both chip designs, data sent off-detector is zero suppressed
- Output data rate ∝ hit rate
- For a strip detector, the strips vary in pitch and number such that occupancy stays even => constant output rate from each chip (**~1.4 Gbit s^{-1}**)
- Not possible for a pixel detector (without serious routing!). Data rate higher towards the beam:
  - 40MHz beam crossing × 5 tracks (inner region) = **200 MHz track rate**
  - Uncompressed data rates of up to 15 Gbit s^{-1}
  - Compressed output of **~12 Gbit s^{-1}** for the hottest ASIC
- In both cases, total detector readout reaches **~2.5 Tbit s^{-1}**



- Two ASIC schemes:
  - **Synchronous readout** - each bunch crossing is processed and data sent out sequentially
  - **Asynchronous readout** - each hit triggers its own readout after charge measurement. Data transmitted out of order, smearing data from several bunch crossings

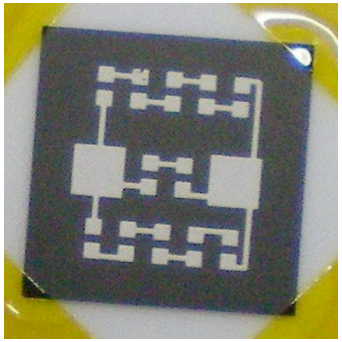
The TELL40 - off detector DAQ

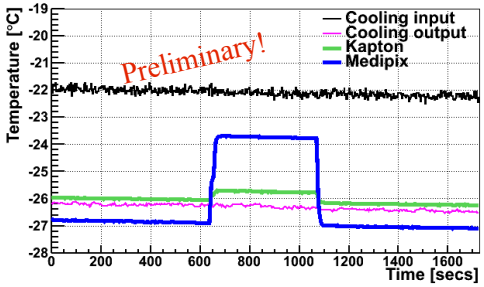


Cooling options

- Cooling of both strips and pixels is challenging
  - Strips must be cooled to the very tip to prevent thermal runaway
  - Pixel chips extend all the way to the tip - heating power directly under the sensor
- Two options being investigated
  - Metallised diamond substrate: traces for chip IO deposited on high conductivity diamond with thermally activated silver paste (only needed for pixels)
  - Microchannel cooling option: overlap with NA62 and ALICE R&D. Must be able to produce ~200µm (wide) × 70µm (deep) channels which can withstand > 100 bar. Several prototypes already produced and working in lab environment 65 bar (at room T) and at -27°C
- Aim to re-use CO_2 cooling system used by the existing detector

Metallised diamond





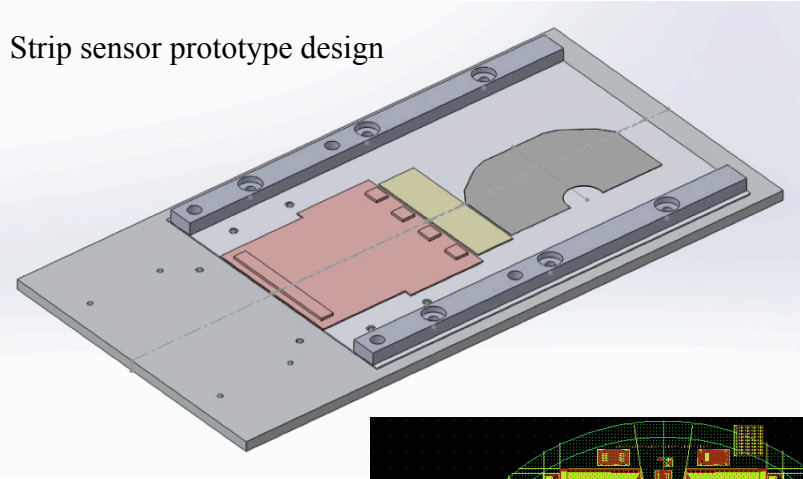
Microchannel cooling prortype performance

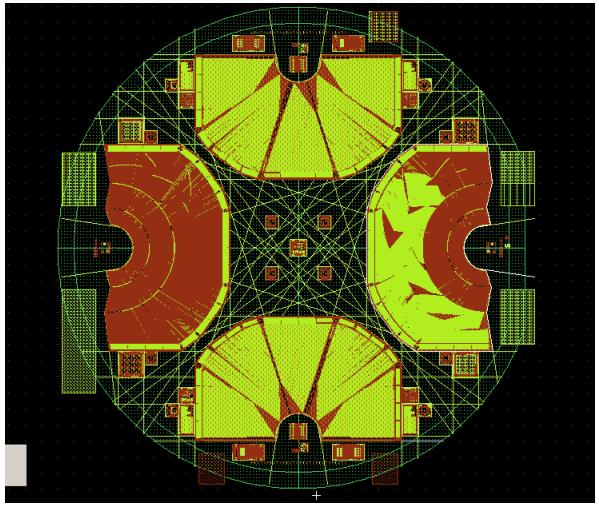
Si microchannels bonded to glass plate

3 chip module

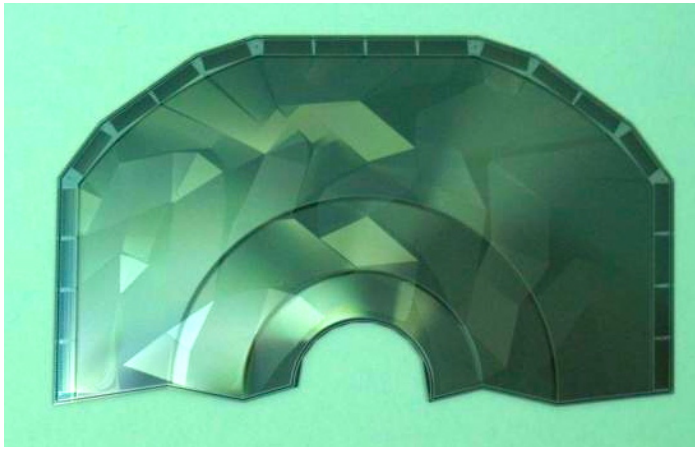
Prototyping - modules

Strip sensor prototype design

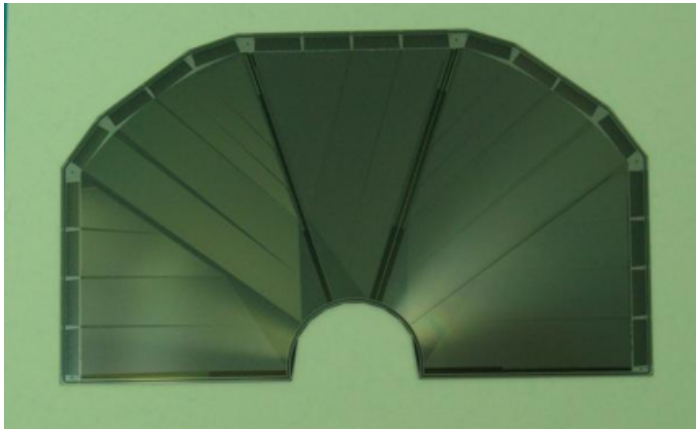




Submitted strip design



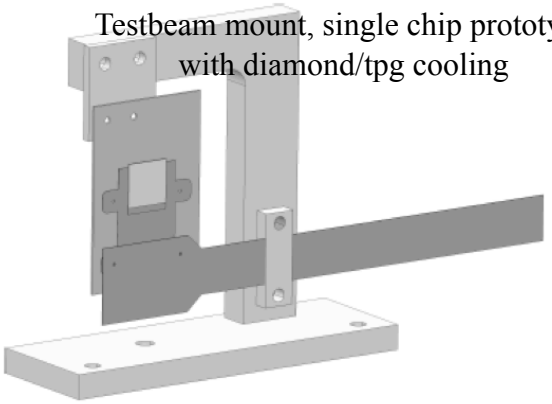
First received Phi sensor



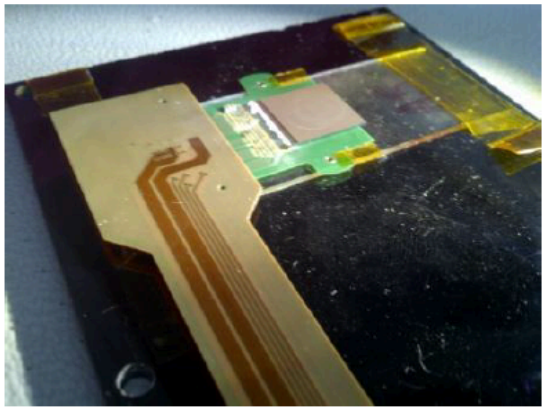
First received R sensor

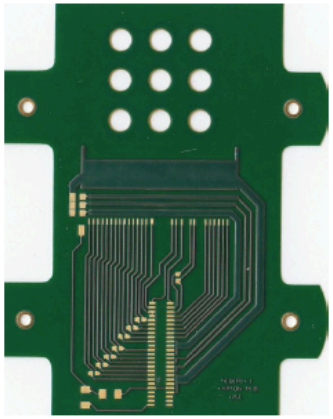
Prototyping - modules

Testbeam mount, single chip prototype with diamond/tpg cooling

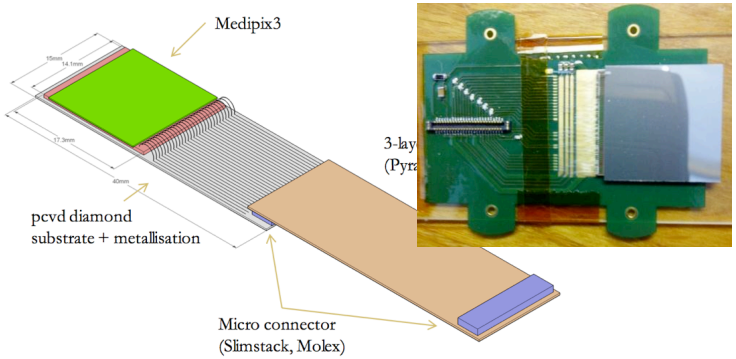


Custom kapton mount and readout flex

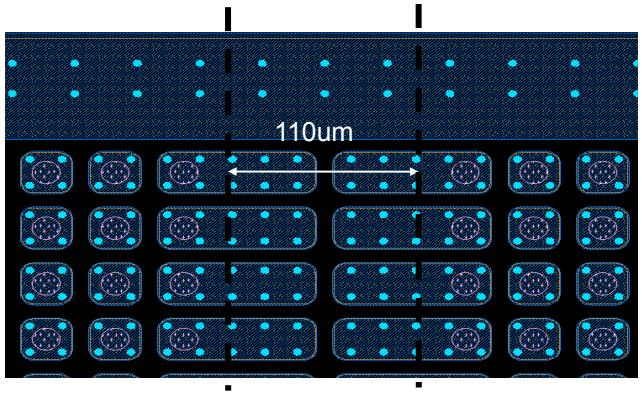




Single chip prototype, conceptual and kapton-mounted in lab



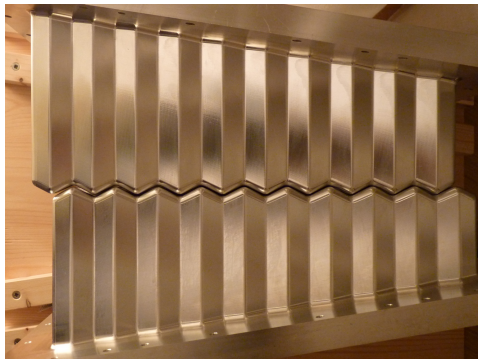
Submitted pixel mask, showing elongated edge pixels



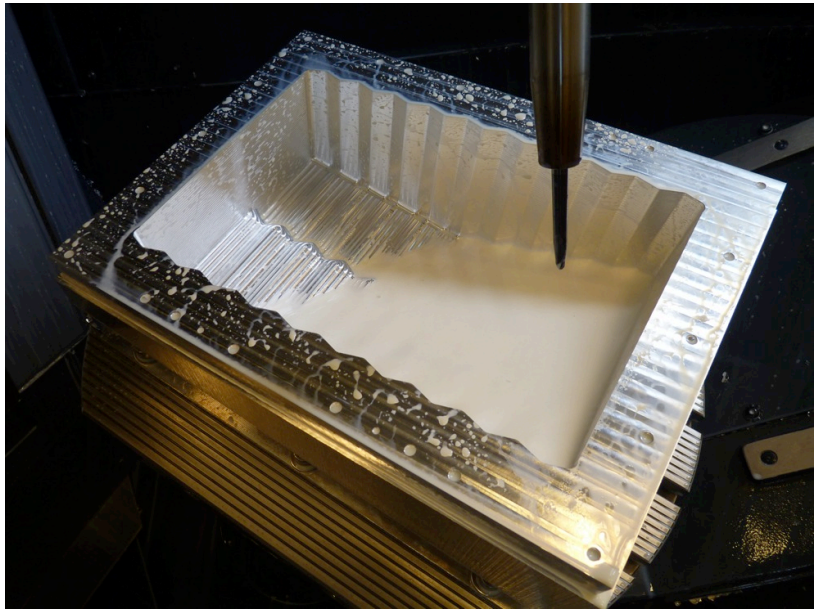
Prototyping - RF foil

- Upgraded VELO will operate in vacuum tank used by current detector
  - Primary beam vacuum separated from secondary vacuum by 200-300µm RF foil
  - Will have to be mechanically stable to cope with pump-down & venting without deformation

- Mill foil from one solid block of material
- 5-axis milling device used
  - Step 1: Mill out the inside
  - Step 2: Fill with wax
  - Step 3: Mill the outside
  - Step 4: Heat and remove wax



Prototype RF foil - two halves



Milling of the RF foil

Testbeam plans

- Testbeam program has been working to test a variety of prototypes. 2012:
  - Performance of 0.5 and 2×10^{15} 1 MeV n_{eq} cm^{-2} irradiated sensors (rad. hard Medipix3)
  - Various guard ring designs with 50 - 2000 μm pixel-to-edge distance and 0 - 6 guard rings
  - Tracking performance of prototype sensors over full θ coverage

- Main priorities for the coming year:
  - **TimePix3:** validate high rate operation (should be able to cope with 40MHz hit pixel rate...) Validate data driven readout style
  - Strip prototypes: Chip tests with low and high intensity beam
  - Sensors: non-uniform irradiation tests, efficiency measurements, signal yield

2013

- TimePix3 tests
- Data driven readout
- High rate operation
- Non-uniform irrad.

→

2014

VeloPix

- Factor 10 rate increase
- 40MHz beam operation

Strip Chip

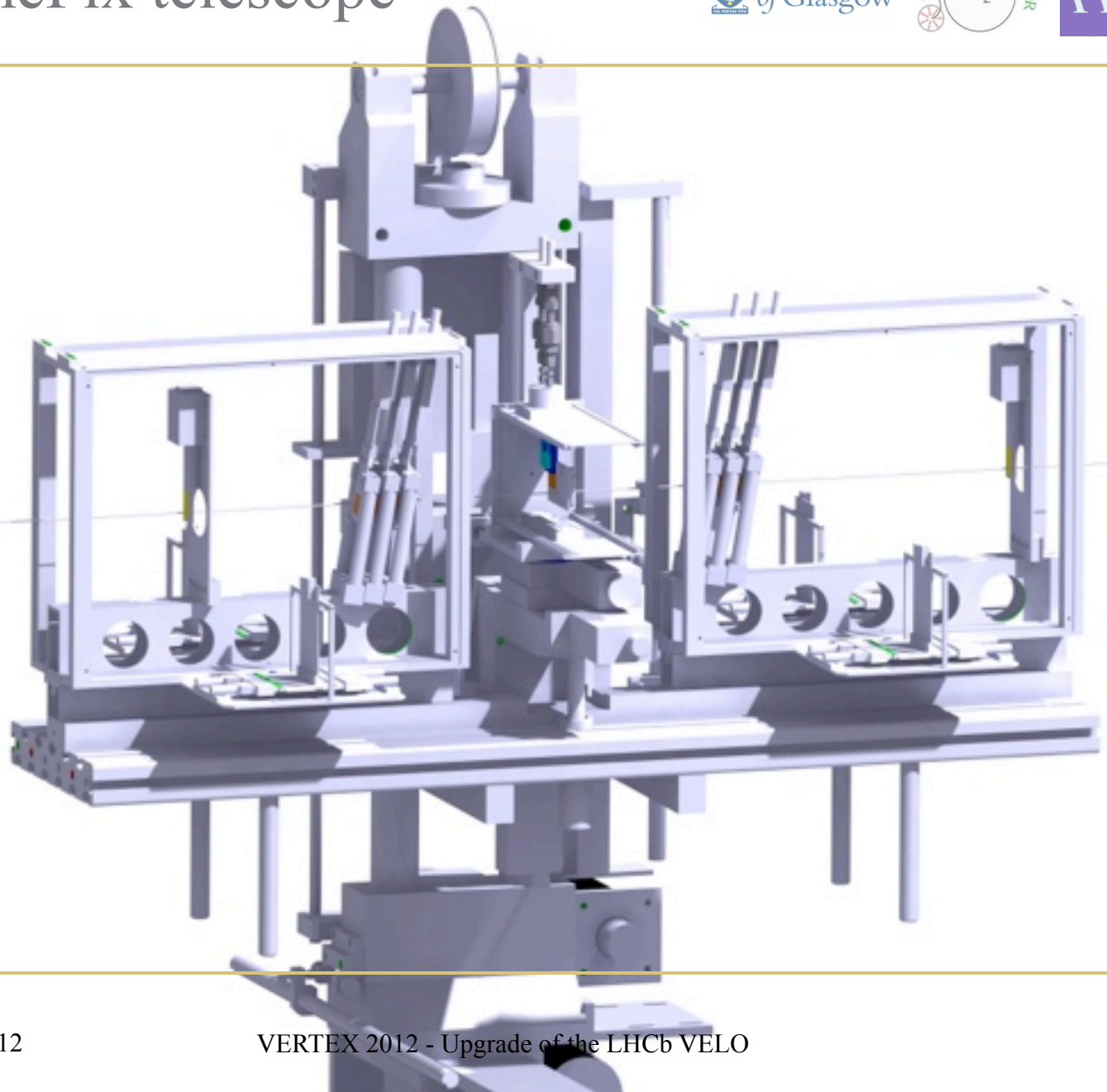
- Low rate operation
- High rate operation
- 40MHz beam operation

→

2015 - 2016

- Full half detector tests?

The TimePix telescope

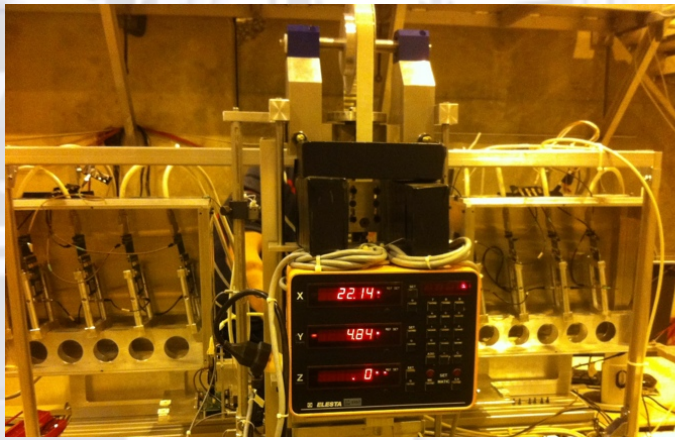


The TimePix telescope

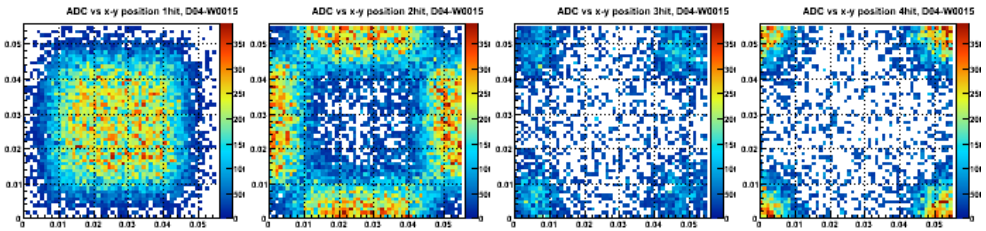
- Development of a high rate precision telescope was necessary to validate TimePix as an option for particle tracking, and to allow a multitude of studies
  - Single hit resolution
  - Efficiency
  - Active area and guard ring structures

- Extension of the telescope as part of the AIDA project - has been used as a test facility by internal (scintillating fibres LHCb upgrade) and external (CLiC, ATLAS PPS, WP9) users

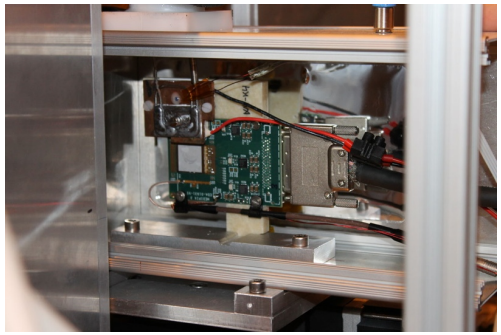
- Performance well characterised:
  - 3 - 12 kHz track rate
  - ~1ns timestamping resolution
  - ~2μm pointing resolution at the DUT
  - Minimal hardware integration



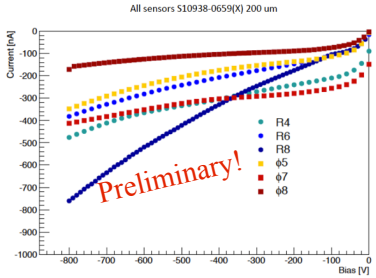
Some brief results...



Charge sharing studies with TimePix chip

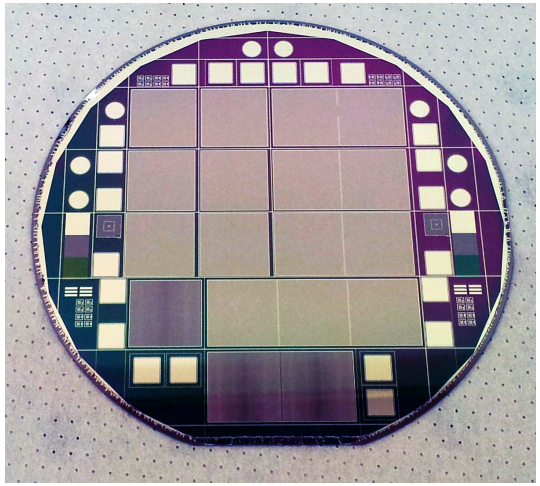


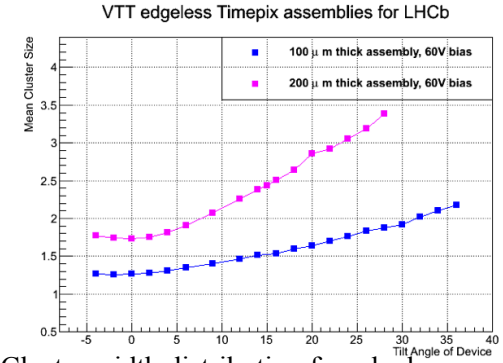
Medipix3 read out with Diamond MERLIN readout (NI PXI-based)



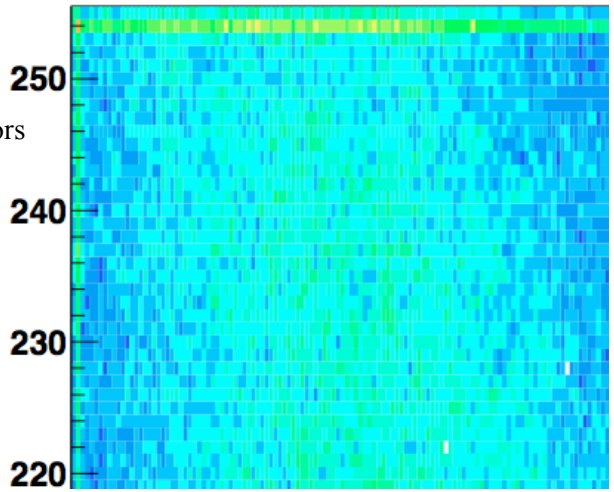
IV curves for prototype strip detectors

Sensor wafer with variable guard ring designs



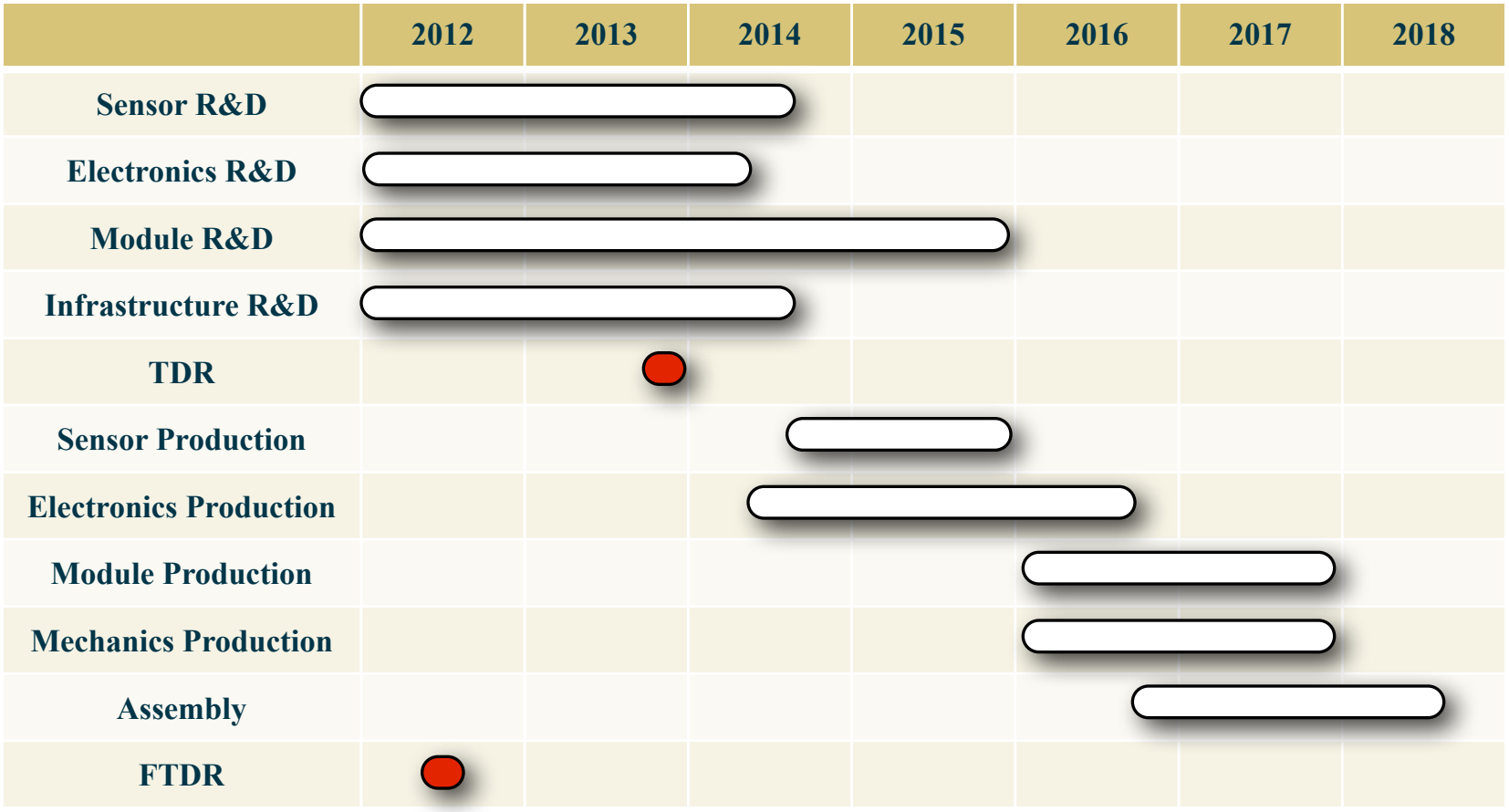


Cluster width distribution for edgeless sensors



ADC weighted hitmap for slim edge pixel sensor showing increased CCE near edge

Timescale


2012
2013
2014
2015
2016
2017
2018
Sensor R&D
Electronics R&D
Module R&D
Infrastructure R&D
TDR
Sensor Production
Electronics Production
Module Production
Mechanics Production
Assembly
FTDR

Conclusions

- Many challenges still to overcome
  - LHCb upgrade scheduled for 2018 - module production 2015/2016
  - R&D programe well underway, with ASIC designs advancing for both options
  - Decisions driven by simulation work and technical feasability
  - Ground details dictated by beam and lab measurements

- Decision over detector type (strip/pixel) to be taken mid-2013
  - Focus resources on most viable option
  - Detailed front end simulation studies

- Timescale is tight (as always)
  - Module production proper to begin in 2016
  - High rate validation 2014 - where?

- Installation during long shutdown in 2018...

- R. Aaij et al. (LHCb Collaboration)

  The LHCb Upgrade

  LHCb (Physics) Public Note LHCb-PUB-2012-010 (July 2012)

- The LHCb Collaboration,

  Framework TDR for the LHCb upgrade

  CERN/LHCC 2012-007, LHCb TDR 12 (May 2012)